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EXAMINER	
SAVLA, ARPAN P	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/820,964	FUJIMOTO ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-39 and 44-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-39 and 44-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/2/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed May 2, 2008 in response to the Office action dated February 2, 2008. Claims 21 and 36-39 have been amended. Claims 40-43 have been canceled. New claims 53-54 have been added. Claims 21-39 and 44-54 are pending in this application.

OBJECTIONS

Claims

1. In view of Applicant's amendments, the objection **claim 21** has been withdrawn.

2. **Claim 53** is objected to because on line 13 of the claim the limitation "first interface **adapters**" should instead read "first interface **units**."

3. **Claim 53** is also objected to because on line 15 of the claim there should be the word "**and**" before the limitation "said processing units."

4. **Claim 54** is objected to because on line 2 of the claim the limitations "first interface" and "second interface" should instead read "first interface **units**" and "second interface **units**" respectively.

5. **Claim 54** is also objected to because on line 3 of the claim the word "subsystem" should instead read "**cluster system**."

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 21-28 and 30-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis et al. (U.S. Patent 6,343,324) (hereinafter "Hubis") in view of Katzman et al. (U.S. Patent 4,228,496) (hereinafter "Katzman").

8. **As per claim 21**, Hubis discloses a storage system comprising:

a plurality of disk drives (col. 7, lines 27-28; Fig. 2, element 108);

at least one logical volume configured by said disk drives (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter having at least one processor and controlling to store data, which are sent from at least one host computer to said logical volume for updating said logical volume, in said disk drives (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180); *It should be noted that the "Processor 180" is analogous to the "processor adapter."*

a plurality of first interface adapters each coupled to said at least one host computer and receiving a write request and data sent from said at least one host computer and sending a first control information related to said write request to at least one of said processor adapters and sending data received at each of said first interface adapters based on a second control information sent from said at least one processor

adapter (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1 – 184-M); *It should be noted that the "I/O Processors 184-1-M" are analogous to the "plurality of first interface adapters."*

a memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186); *It should be noted that the "Data Cache Memory" is analogous to the "memory adapter."*

a plurality of second interface adapters each receiving data stored in said memory adapter from said memory adapter based on a third control information sent from said at least one processor adapter and storing data received at each of said second interface adapters in said disk drives (col. 16, lines 3-6; Fig. 2A, element 185-1); *It should be noted that the "I/O Processors 185-1-M" are analogous to the "plurality of second interface adapters."*

a switch adapter coupled to said processor adapters, said first interface adapters, said memory adapter and said second interface adapters and relaying data between said first interface adapters and said memory adapter and relaying data between said memory adapter and said second interface adapters (col. 15, lines 63-66; Fig. 2A, element 183); *It should be noted that the "PCI Bus Interface and Memory Controller" is analogous to the "switch adapter."*

wherein said switch adapter relays said first and said second control information between said processor adapters and said first interface adapters and relays said third control information between said processor adapters and said second interface

adapters (col. 15, lines 63-66; col. 16, lines 6-9); *It should be noted that the Processor is coupled to the system only through the PCI Bus Interface and Memory Controller, therefore, all control information is required to be relayed via the PCI Bus Interface and Memory Controller.*

Hubis does not disclose a plurality of processor adapters;

wherein the number of said processor adapters are increased or decreased based on a required performance.

Katzman discloses a plurality of processor adapters (col. 13, lines 43-44 and 51-54; Fig. 1, elements 33); *It should be noted that the "processor modules" are analogous to the "processor adapters."*

wherein the number of said processor adapters are increased or decreased based on a required performance (col. 16, line 67 – col. 17, line 3; col. 3, lines 6-15; Fig. 1, elements 33).

Hubis and Katzman are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Katzman's expandable multiprocessor system to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of automatically accommodating additional processors in a

multiprocessing system constructed to accommodate the modular addition of processors as increased computering power is required.

9. **As per claim 22**, the combination of Hubis/Katzman discloses said processor adapters are independently attached to or detached from said first interface adapters (Katzman, col. 16, line 67 – col. 17, line 3; Fig. 1, elements 33 and 41). *It should noted that the "device controllers" are analogous to the "interface adapters."*

10. **As per claim 23**, the combination of Hubis/Katzman discloses said processor adapters are assigned to a process of at least one said first interface adapter and a process of at least one said second interface adapter (Hubis, col. 16, lines 6-9).

11. **As per claim 24**, the combination of Hubis/Katzman discloses said at least one processor adapter is assigned to said plurality of first interface adapters (Hubis, col. 16, lines 6-9).

12. **As per claim 25**, the combination of Hubis/Katzman discloses said at least one processor adapter is assigned to said plurality of second interface adapters (Hubis, col. 16, lines 6-9).

13. **As per claim 26**, the combination of Hubis/Katzman discloses it is possible to increase or decrease the number of said processor adapters in case that the number of said first interface adapters is not increased or decreased (Katzman, col. 16, line 67 – col. 17, line 3; Fig. 1, elements 33 and 41).

14. **As per claim 27**, the combination of Hubis/Katzman discloses it is possible to change the number of said processor adapters on storing data in said disk drives (Katzman, col. 16, line 67 – col. 17, line 3; Fig. 1, elements 33).

15. **As per claim 28**, the combination of Hubis/Katzman discloses the number of said processor adapters is increased or decreased in accordance with the number of said first interface adapters being increased or decreased (Katzman, col. 16, line 67 – col. 17, line 3; Fig. 1, elements 33 and 41).

16. **As per claim 30**, the combination of Hubis/Katzman discloses said first control information is used to notify said at least one processor adapter of receiving said write request (Hubis, col. 15, lines 10-25).

17. **As per claim 31**, the combination of Hubis/Katzman discloses said at least one processor adapter detects an area of said memory in which data of said logical volume need to be stored in accordance with said received first control information (Hubis, col. 15, lines 19-25; col. 16, line 67 – col. 17, line 9). *It should be noted that it is inherently required Processor 180 detect/recognize an area of the Data Cache Memory in order to allocate space for storing data in the Cache Memory during a write task.*

18. **As per claim 32**, the combination of Hubis/Katzman discloses said second control information includes information related to an area of said memory in which data received at said first interface adapter need to be stored (Hubis, col. 15, lines 19-25; col. 16, line 67 – col. 17, line 9). I*t should be noted that it is inherently required Processor 180 allocate/reserve an area of the Data Cache Memory in order to store data in the Cache Memory during a write task.*

19. **As per claim 33**, the combination of Hubis/Katzman discloses said at least one processor adapter finds an area of said disk drives related to said logical volume for

storing data of said logical volume based on said received first control information (Hubis, col. 15, lines 23-25; col. 16, lines 6-9).

20. **As per claim 34**, the combination of Hubis/Katzman discloses said third control information includes information related to an area of said disk drives in which data received at said second interface adapter need to be stored (Hubis, col. 15, lines 23-25; col. 16, lines 6-9).

21. **As per claim 35**, the combination of Hubis/Katzman discloses said at least one processor adapter controls to create a parity data of RAID (Redundant Array of Inexpensive Disks) from data received at least one of said first interface adapters (Hubis, col. 4, line 64 – col. 5, line 3).

22. **As per claim 36**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

at least one logical volume configured by said at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter each having at least one processor and controlling to store data by determining a location at which the data should be stored, the data being sent from said host computer to said logical volume for updating said logical volume, in said disk drive (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer and receiving a write request and data sent from said host computer and sending a first control information related to said write request to said processor adapter and sending data received at

said first interface adapter based on a second control information sent from said processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1); *It should be noted that the "I/O Processor 184-1" is analogous to the "first interface adapter."*

a memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a second interface adapter receiving data stored in said memory adapter from said memory adapter based on a third control information sent from said processor adapter and storing data received at said second interface adapter in said disk drive (col. 16, lines 3-6; Fig. 2A, element 185-1); *It should be noted that the "I/O Processor 185-1" is analogous to the "second interface adapter."*

a switch adapter coupled to said processor adapter, said first interface adapter, said memory adapter and said second interface adapter and relaying said data among said first interface adapter, said memory adapter and said second interface adapter (col. 15, lines 63-66; Fig. 2A, element 183);

wherein said switch adapter relays said first and said second control information between said processor adapter and said first interface adapter and relays said third control information between said processor adapter and said second interface adapter (col. 15, lines 63-66; col. 16, lines 6-9); *It should be noted that the Processor is coupled to the system only through the PCI Bus Interface and Memory Controller, therefore, all*

control information is required to be relayed via the PCI Bus Interface and Memory Controller.

Hubis does not disclose a plurality of processor adapters;

wherein the number of said processor adaptors are increased or decreased based on a required performance, even though the number of said first interface adapter, said memory adapter and said second interface adapter are not increased or decreased.

Katzman discloses a plurality of processor adapters (col. 13, lines 43-44 and 51-54; Fig. 1, elements 33);

wherein the number of said processor adaptors are increased or decreased based on a required performance, even though the number of said first interface adapter, said memory adapter and said second interface adapter are not increased or decreased (col. 16, line 67 – col. 17, line 3; col. 3, lines 6-15; Fig. 1, elements 33 and 41).

Hubis and Katzman are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Katzman's expandable multiprocessor system to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of automatically accommodating additional processors in a

multiprocessing system constructed to accommodate the modular addition of processors as increased computering power is required.

23. **As per claim 37**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

at least one logical volume configured by said at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter having at least one processor and controlling to store data by determining a location at which the data should be stored, the data being sent from said host computer to said logical volume for updating said logical volume, in said disk drive (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer and receiving data sent from said host computer and sending data received at said first interface adapter based on a first control information sent from said processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1);

a memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a second interface adapter receiving data stored in said memory adapter from said memory adapter based on a second control information sent from said processor adapter and storing data received at said second interface adapter in said disk drive (col. 16, lines 3-6; Fig. 2A, element 185-1);

a switch adapter coupled to said processor adapter, said first interface adapter, said memory adapter and said second interface adapter and relaying data of said logical volume among said first interface adapter, said memory adapter and said second interface adapter and not relaying data of said logical volume to said processor adapter (col. 15, lines 63-66; Fig. 2A, element 183); *It should be noted that when the host sends a read request to the logical volumes, Processor 180 does not receive the read data itself, but rather controls the process of sending the read data back to the host.*

wherein said switch adapter relays said first control information between said processor adapter and said first interface adapter and relays said second control information between said processor adapter and said second interface adapter (col. 15, lines 63-66; col. 16, lines 6-9); *It should be noted that the Processor is coupled to the system only through the PCI Bus Interface and Memory Controller, therefore, all control information is required to be relayed via the PCI Bus Interface and Memory Controller.*

Hubis does not disclose a plurality of processor adapters;

wherein it is possible to change the number of said processor adapter on storing on storing data in said disk drives.

Katzman discloses a plurality of processor adapters (col. 13, lines 43-44 and 51-54; Fig. 1, elements 33);

wherein it is possible to change the number of said processor adapter on storing on storing data in said disk drives (col. 16, line 67 – col. 17, line 3; col. 3, lines 6-15; Fig. 1, elements 33).

Hubis and Katzman are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Katzman's expandable multiprocessor system to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of automatically accommodating additional processors in a multiprocessing system constructed to accommodate the modular addition of processors as increased computering power is required.

24. **As per claim 38**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

at least one logical volume configured by said at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter having at least one processor and controlling to store data by determining a location at which the data should be stored, the data being sent from said host computer to said logical volume for updating said logical volume, in said disk drive (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1);

a memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a second interface adapter coupled to said first interface adapter, said processor adapter, and said memory adapter (col. 16, lines 3-6; Fig. 2A, element 185-1);

a switch adapter coupled to said processor adapter, said first interface adapter, said memory adapter and said second interface adapter (col. 15, lines 63-66; Fig. 2A, element 183);

wherein said switch adapter relays data between said first interface adapter and said second interface adapter via said memory adapter among said first interface adapter, said processor adapter, said memory adapter and said second interface adapter based on control information transferred among said first interface adapter, said processor adapter and said second interface adapter of said first interface adapter, said processor adapter, said memory adapter, and said second interface adapter (col. 15, lines 63-66; col. 15, line 67 – col. 16, line; Fig. 2A, elements 183 and 186). *It should be noted that Data Cache Memory buffers any data sent between I/O Processor 184-1 and I/O Processor 185-1.*

Hubis does not disclose a plurality of processor adaptors;

wherein the number of processor adapters are increased or decreased based on a required performance.

Katzman discloses a plurality of processor adapters (col. 13, lines 43-44 and 51-54; Fig. 1, elements 33);

wherein the number of processor adapters are increased or decreased based on a required performance (col. 16, line 67 – col. 17, line 3; ; col. 3, lines 6-15; Fig. 1, elements 33).

Hubis and Katzman are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Katzman's expandable multiprocessor system to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of automatically accommodating additional processors in a multiprocessing system constructed to accommodate the modular addition of processors as increased computering power is required.

25. **As per claim 39**, Hubis discloses a storage system coupled a host computer, said storage system comprising:

at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

at least one logical volume configured by said at least one disk drive (col. 7, lines 27-28; Fig. 2, element 108);

a processor adapter having at least one processor and controlling to store data by determining a location at which the data should be stored, the data being sent from said host computer to said logical volume for updating said logical volume, in said disk drive (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a first interface adapter coupled to said host computer and receiving a write request and data sent from said host computer and sending a first control information related to said write request to said processor adapter and sending data received at said first interface adapter based on a second control information sent from said processor adapter (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1);

a memory adapter having at least one memory, said memory temporarily storing data sent from said first interface adapter (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a second interface adapter receiving data stored in said memory adapter from said memory adapter based on a third control information sent from said processor adapter and storing data received at said second interface adapter in said disk drive (col. 16, lines 3-6; Fig. 2A, element 185-1);

wherein said processor adapter coupled to said first interface adapter and said second interface adapter and sends said second control information to said first interface adapter and sends said third control information to said second interface adapter (col. 16, lines 6-9);

wherein said first interface adapter sends data to said memory adapter among said processor adapter, said memory adapter and said second interface adapter (col. 15, line 67 – col. 16, line 3);

wherein said second interface adapter receives data from said memory adapter among said processor adapter, said memory adapter and said first interface adapter (col. 16, lines 3-6);

wherein said memory adapter receives data from said first interface adapter and said second interface adapter among said processor adapter, said first interface adapter and said second interface adapter (col. 15, line 67 – col. 16, line 6);

Hubis does not disclose a plurality of processor adaptors;

wherein the number of processor adapters are increased or decreased based on a required performance.

Katzman discloses a plurality of processor adapters (col. 13, lines 43-44 and 51-54; Fig. 1, elements 33);

wherein the number of processor adapters are increased or decreased based on a required performance (col. 16, line 67 – col. 17, line 3; ; col. 3, lines 6-15; Fig. 1, elements 33).

Hubis and Katzman are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Katzman's expandable multiprocessor system to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of automatically accommodating additional processors in a

multiprocessing system constructed to accommodate the modular addition of processors as increased computering power is required.

26. **As per claims 44-52**, the combination of Hubis/Katzman discloses the memory adapter includes a control information memory module in which information for controlling data transfer is stored (Hubis, col. 15, line 67 – col. 16, line 3; col. 8, lines 2-5; Fig. 2A, element 186).

27. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis in view of Katzman as applied to claim 21 above, and further in view of Kuchta et al. (U.S. Patent 6,014,319) (hereinafter "Kuchta").

28. **As per claim 29**, the combination of Hubis/Katzman does not disclose a first portion of said processor adapters are assigned to a process of at least one of said first interface adapters;

a second portion of said processor adapters are assigned to a process of at least one of said second interface adapters;

a proportion between said first portion and said second portion is decided in accordance with a proportion between a performance of said at least one first interface adapter and a performance of said at least one second interface adapter.

Kutcha discloses a first portion of said processor adapters are assigned to a process of at least one of said first interface adapters (col. 7, lines 15-18; Fig. 2A, element 245; Fig. 2B, elements 211-212); *It should be noted that "I/O modules 211-212" are analogous to the "first portion of processor adapters" and "I/O cards 245" are analogous to "first interface adapters."*

a second portion of said processor adapters are assigned to a process of at least one of said second interface adapters (col. 7, lines 35-38; Fig. 2A, element 246; Fig. 2B, elements 209-210); *It should be noted that "I/O modules 209-210" are analogous to the "second portion of processor adapters" and "I/O cards 246" are analogous to "second interface adapters."*

a proportion between said first portion and said second portion is decided in accordance with a proportion between a performance of said at least one first interface adapter and a performance of said at least one second interface adapter (col. 5, lines 59-63). *It should be noted that amount of I/O modules 209-210 versus the amount of I/O modules 211-212 (i.e. a proportion between said first portion and said second portion) is based on performance characteristics.*

The combination of Hubis/Katzman and Kuchta are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Kuchta's additional I/O modules within Hubis/Katzman's storage system.

The motivation for doing so would have been to provide later system enhancements (Kuchta, col. 5, lines 49-50).

29. Claims 53 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis in view of Katzman and Matsunami et al. (U.S. Patent Application Publication 2002/0091898) (hereinafter "Matsunami").

30. **As per claim 53**, Hubis discloses a storage system comprising:

a plurality of disk drives (col. 7, lines 27-28; Fig. 2, element 108);

a plurality of first interface units each coupled to said at least one host computer and receiving a write request and data sent from said at least one host computer (col. 7, line 64 – col. 8, line 5; col. 15, lines 19-25; col. 15, line 67 – col. 16, line 3; Fig. 2A, element 184-1 – 184-M);

a plurality of second interface units each coupled to said plurality of disk drives (col. 16, lines 3-6; Fig. 2A, element 185-1);

a processor unit separated from said first interface units and said second interface units and each having at least one processor (col. 15, line 67 – col. 16, line 9; Fig. 2A, element 180);

a memory unit having at least one memory, said memory temporarily storing data sent from said first interface units (col. 15, line 67 – col. 16, line 3; Fig. 2A, element 186);

a switch unit coupled to said first interface units, said second interface units, and said processor units (col. 15, lines 63-66; Fig. 2A, element 183).

Hubis does not disclose a storage system comprising a first cluster system and a second cluster system,

a plurality of processor units;

wherein the switch unit of the first cluster system is coupled to the switch of the second cluster system by a communication path;

wherein the number of said processor units of the first cluster system and said second cluster system can be increased or decreased based on a required performance.

Katzman discloses a plurality of processor units (col. 13, lines 43-44 and 51-54; Fig. 1, elements 33);

wherein the number of said processor units can be increased or decreased based on a required performance (col. 16, line 67 – col. 17, line 3; col. 3, lines 6-15; Fig. 1, elements 33).

Hubis and Katzman are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to apply Katzman's expandable multiprocessor system to Hubis' storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of automatically accommodating additional processors in a multiprocessing system constructed to accommodate the modular addition of processors as increased computering power is required.

The combination of Hubis/Katzman does not disclose a storage system comprising a first cluster system and a second cluster system,

wherein the switch unit of the first cluster system is coupled to the switch of the second cluster system by a communication path.

Matsunami discloses a storage system comprising a first cluster system and a second cluster system (paragraph 0043; paragraph 0070; Fig. 14, elements 10 and 20); *It should be noted that each "disk array switch" combined with its respective "disk array subset" comprises a "cluster."*

wherein the switch unit of the first cluster system is coupled to the switch of the second cluster system by a communication path (paragraph 0043; paragraph 0070; Fig. 3, elements 201 and 2040; Fig. 14, element 2040). *It should be noted that the "crossbar switch" is analogous to the "switch unit" and the "Intercluster I/F" is analogous to the "communication path."*

The combination of Hubis/Katzman and Matsunami are analogous art because they are from the same field of endeavor, that being storage systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Matsunami's clustered storage system and Hubis/Katzman's array controller and processor modules such that the storage system comprises a first cluster and a second cluster, each cluster comprising an array controller, a plurality of processor modules, and a plurality of disk drives, because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of providing a disk storage system that responds easily to needs for high reliability and future expansion.

31. **As per claim 54**, the combination of Hubis/Katzman/Matsunami discloses said processor units in said first cluster system can instruct said plurality of first interface

units and the plurality of second interface units of said second cluster system to transfer a data (Matsunami, paragraph 0070).

Response to Arguments

32. Applicant's arguments filed May 2, 2008 with respect to **claims 21-39 and 44-54** have been fully considered but they are not persuasive.

33. With respect to Applicant's argument regarding Katzman's processor modules, on page 17 of the communication filed May 2, 2008, the Examiner respectfully disagrees. Firstly, it is noted that Applicant's assertion that "Element 33 of Katzman is included in a host computer" (see page 17) is in error. Nowhere in Katzman does it mention a "host" much less a "host computer." Katzman's processor modules (i.e. element 33) are included in multiprocessor system 31.

Secondly, It is noted that the feature upon which Applicant relies (i.e., "processor unit in a storage device") is not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Lastly, assuming, *in arguendo*, that the claims actually disclose that the "processor units/adapters" are in a "storage device" Katzman still discloses such a limitation. As can be seen from Fig. 1 of Katzman, processor modules 33 (i.e. processor units/adapters) are included in multiprocessor system 31. As can also be seen from Fig. 1 of Katzman, multiprocessor system 31 also includes discs 45, thus, multiprocessor system 31 is a "device" that "stores" data. Therefore, when taking a

broad and reasonable interpretation of the limitation "storage device", it logically follows that Katzman's multiprocessor system 31 constitutes a "storage device." As mentioned earlier, in Katzman processor modules 33 are in multiprocessor system 31. Consequently, Katzman discloses processor units/adapters ("processor modules 33") in a storage device ("multiprocessor system 31"). Accordingly, Katzman's processor modules sufficiently equate to Applicant's processor units/adapters.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 21-39 and 44-54** have received a second action on the merits and are subject of a second action final.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571)272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan Savla/

August 13, 2008
Examiner, Art Unit 2185

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185